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In the United States Patent and Trademark Office

Date: April 8, 2002

In re Application of: R. T. Bailis, et al.

Serial Number: 10/016,449 ***Filed:*** Dec. 10, 2001

For: **METHOD AND SYSTEM FOR USE OF A FIELD PROGRAMMABLE GATE ARRAY (FPGA) FUNCTION WITHIN AN APPLICATION SPECIFIC INTEGRATED CIRCUIT (ASIC) TO ENABLE CREATION OF A DEBUGGER CLIENT WITHIN THE ASIC**

Group Art Unit: 2133

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Assistant Commissioner of Patents
Washington, DC 20231

TRANSMITTAL OF FORMAL DRAWINGS

Attached please find formal drawings (3 sheets) for the above-identified application.

Respectfully submitted,

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I hereby certify this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks; Washington, DC 20231

Date: April 11, 2002

Karen Orzechowski
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